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Attorney Docket No. TI-30961

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventor(s): Cho, et al

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Irish Paramore

For: **AUTOMATIC BIT-RATE DETECTION SCHEME FOR USE ON SONET TRANSCEIVER**

Enclosed are:

6 Sheets of drawings and 14 pages of Specification (including Abstract)
X Declaration/Power of Attorney
X Assignment with form PTO 1595

FEE CALCULATION					FEE
	NUMBER		**NUMBER EXTRA**	**RATE**	**BASIC FEE $ 710.00**
Total Claims	30	-20 =	10	X $18 =	180.00
Independent Claims	4	- 3 =	1	X $80 =	80.00
				Total Filing Fee	$ 970.00

Please charge Deposit Account No. 20-0668 in the amount of the Total Fees set forth. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-0668.

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AUTOMATIC BIT-RATE DETECTION SCHEME

FOR USE ON SONET TRANSCEIVER

FIELD OF THE INVENTION

The present invention is generally related to SONET/SDH communication networks, and more particularly to transceivers and methods of use in SONET/SDH networks.

BACKGROUND OF THE INVENTION

High speed synchronous optical communication networks are typically referred to as SONET/SDH networks. Conventionally, SONET/SDH transceivers transmit and receive at the same data rate. Thus, two SONET/SDH transceivers communicating with each other over an optical fiber link need to be configurable to operate at the same data speed, which can vary. This variable data rate requires that a machine or technician be able to configure the speed the two transceivers can communicate with each other at.

Typically, these SONET/SDH transmission equipment contain an input/output (IO) card that is designed to operate at particular operating data rate frequency. This maximum operating data rate frequency is primarily established and limited by the semiconductor transceiver devices comprising the transmitter and receiver and being designed for a specific data rate frequency.

In one conventional solution, outlined in an article entitled "A 0.155-,0.622-, and 2.488-Gb/s Automatic Bit-Rate Selecting Clock and Data Recovery IC for Bit-Rate Transparent SDH Systems" authored by J.C. Scheytt, G. Hanke and U. Langmann published in the December 1999 issue of IEEE Journal of Solid-State Circuits, there is described a system that provides an automatic bit-rate transceiver. This article describes the use of two clocking rates, analog elements i.e. low pass filter, threshold voltage generator, and voltage comparitor, relying on the relative frequency of the data edges. This transceiver circuit, disadvantageously, takes milliseconds to switch between different received data bit rates.

There is desired an improved SONET/SDH transceiver that is able to detect and receive data automatically and quickly, to set itself to operate at the highest and correct data rate frequency. The desired improvement would hopefully only use one clocking frequency, that is all digital, and requires significantly less time to detect and adjust to a new data bit rate.

SUMMARY OF THE INVENTION

The present invention achieves technical advantages as an automatic bit-rate detection scheme for use in SONET/SDH transceivers that uses only one clocking frequency, is all digital, and requires less than 250 microseconds to detect and synchronize to a received data bit-rate.

The present invention achieves these technical advantages by ascertaining and analyzing events that are guaranteed to be present in all SONET/SDH data streams. A1 and A2 framing bytes occur at 125 microseconds intervals in all SONET/SDH signals. The transitions of these bits in the framing bytes represent the minimum transition intervals of the received data. The present invention examines this transition interval to measure the bit data rate and determine the operating frequency of the received data. A series of flip-flops are used to clock in the A1 and A2 framing bytes at the maximum possible data bit-rate. A set of static combinational byte-logic circuits are used to detect specific data-bit patterns which appear in the A1 and A2 SONET framing bytes. Each combinational circuit looks for a pattern occurring at a specific

communication rate. Latches capture the pulses that are generated by the combinational circuits each time that the pattern is detected. After a sufficient predetermined time has passed, the output of the capturing latches indicates which bit-rates have been detected. A multi-rate transceiver chip is then responsively set to operate at the highest rate detected.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram overview of a SONET communication link having a multi bit-rate SONET transceiver at each end;

Figure 2 illustrates the timing of the A1 and A2 framing bytes occurring at 125 microsecond intervals;

Figure 3 is a schematic of a set of flip-flops used to serially clock in the arriving framing byte data and which flip-flops are clocked at the fastest bit-rate possible;

Figure 4 is a schematic of the rate detect circuit illustrated in Figure 3 according to the present invention including combinational circuits detecting data patterns to ascertain the bit-rate of the incoming data; and

Figure 5 is a schematic of a second embodiment of the invention including a rate detection circuit adapted to analyze parallized data.

DETAIL DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to Figure 1 there is illustrated generally at 10 a SONET optical communication link having an optical transceiver 12 at one end and an optical transceiver 14 at

the other end communicating with one another over an optical fiber link generally shown at 16. In one illustrative case, but with no limitation to this data rate being intended, transceiver 12 will initiate data communications with receiving transceiver 14 at a data bit-rate which can be, for instance, 2.488 Gb/s (OC-48), 1.244 Gb/s (OC-24) (half maximum data bit-rate), or .622 Gb/s (OC-12) (1/4 maximum data bit-rate). It is envisioned higher data rates can be provided and utilized such as those based on OC-192, OC-768 and so on. However, the receiving transceiver 14 will not initially know the data bit-rate of incoming data. According to the present invention, ascertaining this data bit-rate, quickly and accurately, using a single clock is achieved such that the receiving transceiver 14 can quickly be set to the data bit-rate and communicate back with transceiver 12 at this ascertained bit-rate. Each transceiver 12 and 14 is seen to comprise a transmitter 18 and a receiver 19.

Referring to Figure 2, there is illustrated at 20 that all SONET signals have A1 and A2 framing bytes shown at 22 and 24, respectively as part or subset of the data string shown in Figure 2 occurring at 125 microsecond intervals. The framing bytes have bits represented as;

A1 = 11110110 (F6h)

A2 = 00101000 (28h)

These bits are transmitted unscrambled so that these framing bits represent the minimum transition intervals of the data corresponding to the maximum data bit-rate or data frequency. The present invention examines these framing and other bytes to quickly and accurately measure the data bit-rate and determine the operating frequency of the incoming received data. The "101" and "010" bit sequence portion of these A1 and A2 framing bytes are searched, the presence of which when detected is indicative of and corresponds to a minimum bit-rate.

Referring now to Figure 3, there is illustrated at 30 an automatic bit-rate detection circuit comprising a portion of transceiver 14. A set of flip-flop devices 32 that are used to serially clock in the arriving bits of the A1 and A2 framing bytes. This arriving framing bits are provided to input 34 of the first flip-flop 32 shown at left. The maximum clock rate (clk) of

clock 36, in this example, operating at 2.488 Gb/s, clocks the framing bits from input 34 through the set of flip-flops 32. It the actual incoming data bit-rate is the maximum data rate and clock speed, i.e. 2.488 Gbls, each bit will be clocked into one flip-flop 32. If the actual incoming data bit-rate is ½ of the maximum data rate and clock speed, i.e. 1.244 Gb/s, each bit will be clocked into two (2) flip-flops 32. Likewise, if the incoming data bit-rate is received at ¼ the maximum data rate, i.e. .622 Gb/s, each bit of the framing data will be clocked into four (4) flip-flops 32.

The output of each flip-flop 32 is provided on data lines 40 to a rate detect circuit 50 according to the present invention. These data bits are provided in parallel to the logic circuit 50 and are represented as data bits do(1), do(3), do(4), do(5), do(6) and do(7). Initially, the flip-flops 32 are in the reset condition.

Referring now to Figure 4, there is illustrated in more detail the rate detect circuit 50 shown in Figure 3. Shown in Figure 4 is a plurality of combinational logic circuits each having inputs connected to a unique set of nodes between flip-flops 32 and receiving the clocked output data from the respective flip-flops 32 in Figure 3. Shown at 70 is a first combinational logic group having a pair of 4-input NAND gates 72 receiving a first set of data bits data do(7), do(6), do(5) and do(4). The NAND gates are logically connected to look for a 1010 or 0101 data pattern in the framing bytes A1 and A2. If either of these data bit patterns appear, the received framing data clocked into circuit 50 is determined to must be switching at the same rate as the clock 36, i.e. 2.488 Gb/s. Accordingly, and responsively, the combinational circuit 70 generates a logic 1 pulse at output 74 thereof, and a first D flip-flop shown at 76 will have a logic low at its inverting output 4.

Similarly, a second combinational logic circuit shown at 80 has a pair of 3-input NAND gates 82 looking at a second set of input data bits do(7), do(5), and do(3) and looking for a 101 or 010 data-bit pattern in the framing bytes A1 and A2. If either of these data bit patterns appears, the incoming framing bytes data bits are determined to possibly, but not necessarily, be switching at ½ the maximum clock rate, i.e. 1.244 Gb/s. Accordingly, this combinational logic

circuit 80 generates a logic at output 84, 1 pulse that will cause corresponding a D flip-flop shown at 86 to have a low value at its inverting output.

Shown at 90 is a third combinational logic circuit having a pair of 4-input NAND logic gates 92 looking at third set of input data bits do(7), do(5), do(3) and do(1) and looking for a data bit pattern 1001 or 0110. If this data bit sequence is detected, it is determined that the input data rate of the framing data A1 and A2 may be switching at 1/4 the maximum clock rate i.e. .622 Gb/s. Accordingly, this combinational circuit 90 generates a logic 1 pulse at or about 94 that will cause a D flip-flop 96 to have a low value at its inverting output.

A combinational circuit shown at 100 monitors the outputs of logic circuits 76, 86 and 96, as shown, whereby the following data shown in Table 1 is generated:

TABLE 1

RSEL 0_OUT	RSEL 1_ OUT	INDICATION
0	0	FF 1 is high
1	0	FF2 is high and FF1 is low
0	1	FF3 is high, and FF1 and FF2 are low
1	1	FF1, FF2, and FF3 outputs are low

After 250 microseconds is determined to have passed since the inception of receiving data, which is sufficient for at least one SONET framing byte that is 125 microseconds long to have been received, these results are held by logic circuit 100 at outputs RSEL 0_OUT and RSEL 1_OUT. These outputs are sampled by logic circuitry 52 which determines using Table 1 which data bit-rate is being received as a function of these two outputs, and providing a logic output signal indicative of this received data bit-rate to transceiver 14. Transmitter 18 or Transceiver 14 then is able to communicate with transceiver 12 at the determined data bit-rate, automatically.

Knowing the predetermined data bit patterns of the bits in the A1 and A2 framing bytes, which again, is common in all SONET signals regardless of the data communication bit rate, allows the logic circuitry 50 to sample this data to search for the "101" or "010" bit sequence at the highest possible data bit rate, and thus ascertain the data-bit-rate. The D flip-flops 32 provide nodes which allow the combinational circuit to sample data of the flip-flops 32 and to determine the data bit-rate. For instance, with regards to the framing byte A1, if data is received at ½ the maximum data rate, every bit of the framing byte will be clocked into two (2) flip-flops 32. This is the same for the bits of the A2 framing byte.

Similarly, if incoming framing data is received at ¼ the maximum data rate, i.e., .622 Gb/s in this example, each framing bit of the framing bytes will be clocked into four of the flip-flops 32. Thus, for instance, the first bit being a logic "1" of framing byte A1 is clocked through the first four D flip-flops 32 such that a logic 1 is provided at outputs do(7), do(6), do(5) and do(4). However, the logic circuit 56 clocks (samples) this data in at the maximum data rate of 2.44 Gb/s. The framing bits of both framing bytes are eventually clocked through the flip-flops 32, and the combinational logic circuits sample and detect the bit sequence, where the "101" or "010" bit patterns of the framing bytes are screened for the entire framing bytes. After 250 microseconds have past, again, sufficient for at least one of the SONET frame bytes to have been received and clocked through the flip-flops 32, the outputs at the respective combination logic circuits 70, 80 and 90 are provided to the combinational circuits 76, 86 and 96, respectively, and the combinational circuit 100.

Referring now to Figure 5, there is shown a schematic of a circuit that can detect a data rate of parallized data. By way of illustration, but without any intended limitation, data parallelized into a 4-bit bus will be discussed for clarity and understanding of this embodiment.

The data comes into this circuit 100 in the form of a 4-bit bus. The task is to extract the "101" or "010" from the framing bytes of this data stream. The clock that drives these flip-flops no longer needs to be at the highest possible frequency of the data stream we want to detect. Rather, the clock CLK, in this example, runs at ¼ the highest possible data rate to be detected. The limitation is that, now, the "101" or "010" bit pattern could be hiding in one of several positions.

Looking at the case for the highest incoming rate, if we represent the data in serial manner, the bits would have come in as:

A3 A2 A1 A0 B3 B2 B1 → direction of data stream

Note: this data stream matches the Q output label of the flip-flops.

The "101" or "010" bit pattern could be in:

(A3,A2,A1) or (A2,A1,A0) or (A1,A0,B3) or (A0,B3,B2)

Thus, the combinational logic 102 needed to detect the "101" or "010" bit pattern becomes more complicated, as illustrated.

For the lower bit-rate cases, such as a received data bit-rate at ½ max rate data rate, the bit pattern we look for is "110011" or "001100". Since there are consecutive 0's and 1's the bits we observe get reduced, and this is taken advantage of in the circuit shown on Figure 5.

Though the invention has been described with respect to a specific preferred embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present application. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.

WE CLAIM:

1. A bit-rate detection circuit, comprising:

a plurality of shift registers adapted to serially shift in bits of data having a data frequency from a first transceiver, said shift registers being clocked at a first predetermined rate; and

logic circuitry responsively coupled to said shift registers providing an output signal indicative of the data frequency.

2. The bit-rate detection circuit of Claim 1 wherein said first predetermined rate is the highest possible data rate that the incoming data frequency can be.

3. The bit-rate detection circuit of Claim 1 wherein said logic circuitry is coupled to nodes defined between said shift registers.

4. The bit-rate detection circuit of Claim 3 wherein said logic circuitry comprises a first logic set and a second logic set each providing an output signal, said first logic set being coupled to a first set of said nodes between said shift registers, and said second logic set being coupled to a second set of said nodes between said shift registers.

5. The bit-rate detection circuit of Claim 4 wherein said first logic set determines if said incoming data frequency is a first predetermined frequency, and said second logic set determines if said incoming data frequency is a second predetermined frequency being less than said first predetermined frequency.

6. The bit-rate detection circuit of Claim 5 wherein said first predetermined frequency is a multiple of said second predetermined frequency.

7. The bit-rate detection circuit of Claim 4 further comprising output logic circuitry responsively coupled to said first logic set and said second logic set, said output logic circuitry providing said output signal indicative of the data frequency.

8. The bit-rate detection circuit of Claim 4 further comprising a third logic set coupled to a third set of said nodes being different than said first and second sets of nodes.

9. The bit-rate detection circuit of Claim 8 wherein said third logic set determines if said incoming data frequency is a third predetermined frequency being less than said second predetermined frequency.

10. The bit-rate detection circuit of Claim 9 wherein said first predetermined frequency is in multiple of said third predetermined frequency.

11. The bit-rate detection circuit of Claim 10 wherein said third predetermined frequency is also a multiple of said second predetermined frequency.

12. The bit-rate detection circuit of Claim 1 further comprising a communications transceiver module responsively coupled to said logic circuitry output signal and adapted to transmit data back to said first transceiver at said incoming data frequency.

13. The bit-rate detection circuit of Claim 1 wherein said logic circuitry includes a single clock operating at a first frequency.

14. The bit-rate detection circuit of Claim 1 wherein said logic circuit provides said output signal as a function of framing data clocked into said shift registers.

15. The bit-rate detection circuit of Claim 14 wherein said framing data is A1 and A2 SONET framing bytes.

16. A data transceiver, comprising:

a data receiver circuit;

logic circuitry responsively coupled to said receiver circuit determining a data rate of data received by said data receiver, said logic circuit including and operating off a single clock operating at a first predetermined frequency; and

a data transmitter responsively coupled to said logic circuitry and adapted to transmit data at a data rate as a function of said output signal.

17. The bit-rate detection circuit of Claim 16 wherein said logic circuitry comprises;

a plurality of shift registers adapted to serially shift in data having a data frequency from a first transceiver, said shift registers being clocked at a first predetermined rate; and

logic circuitry responsively coupled to said shift registers providing an output signal indicative of the incoming data frequency.

18. The bit-rate detection circuit of Claim 17 wherein said first predetermined rate is the highest possible data rate that the incoming data frequency can be.

19. The bit-rate detection circuit of Claim 17 wherein said logic circuitry is coupled to nodes defined between said shift registers.

20. The bit-rate detection circuit of Claim 19 wherein said logic circuitry comprises a first logic set and a second logic set each providing an output signal, said first logic set being coupled to a first set of said nodes defined between said shift registers, and said second logic set being coupled to a second set of said nodes defined between said shift registers.

21. A method of detecting a bit-rate of data incoming to a receiver, comprising the steps of:

a) clocking said incoming bit data at a first frequency into a plurality of shift registers having a node between each said shift register; and

b) analyzing data at a plurality of said nodes to determine the bit-rate of said incoming bit data.

22. The method as specified in Claim 21 wherein said first frequency is the maximum possible data bit-rate of said incoming bit data.

23. The method as specified in Claim 22 wherein logic circuitry analyzes said bit data, said logic circuitry having a first logic set coupled to a first set of said nodes determining if said data bit-rate could be a first data rate, and a second logic set coupled to a second set of said determining if said data bit-rate could be a second data rate being less than said first data rate.

24. The method of Claim 23 wherein said first data rate is said first frequency, and said first data rate is also a multiple of said second data rate.

25. The method of Claim 21 further comprising the step of responsively transmitting data from a transmitter at a data rate being said determined incoming data bit-rate.

26. The method of Claim 21 wherein frame data is said analyzed data in said step b).

27. The method of Claim 26 where in said frame data is a A1 and A2 SONET framing byte .

28. A bit-rate detection circuit, comprising:

a plurality of shift registers adapted to shift in bits of data having a data rate in parallel from a first transceiver, said shift registers being clocked at a predetermined clock rate; and

logic circuitry responsively coupled to said shift registers providing an output signal indicative of the data rate.

29. The bit-rate detection circuit as specified in Claim 28, wherein said clock rate is less than the maximum data rate.

30. The bit-rate detection circuit as specified in Claim 29, wherein said data rate is a multiple of said clock rate.

ABSTRACT

An automatic bit-rate detection scheme (30) for use in SONET/SDH transceivers (12, 14) that uses only one clocking frequency (clk), is all digital, and requires less than 250 microseconds to detect a new data bit-rate. The present invention analyzes events that are guaranteed to be present in all SONET data streams. A1 and A2 framing bytes (22,24) occur at 125 microseconds intervals in all SONET signals. The bit transitions in the framing bytes represent the minimum transition intervals of the received data. The present invention examines this bit interval to determine the operating frequency of the received data. A set of combinational logic circuits (70, 80, 90) are used to detect specific data bit patterns which appear in the A1 and A2 SONET framing bytes, such as "010" and "101". The combinational circuit looks for specific patterns of data bits occurring at a specific communication rate. Latches (76, 86, 96) capture the pulses that are generated by the combinational circuits each time that the particular bit pattern is detected. After sufficient time is passed, the output of the capturing latches indicates which data rates have been detected and logic determines the received data bit-rate, (52, 100). A multi-rate chip is then responsively set to communicate at the highest rate detected. The data can be shifted in serially or in parallel.

TI-30961

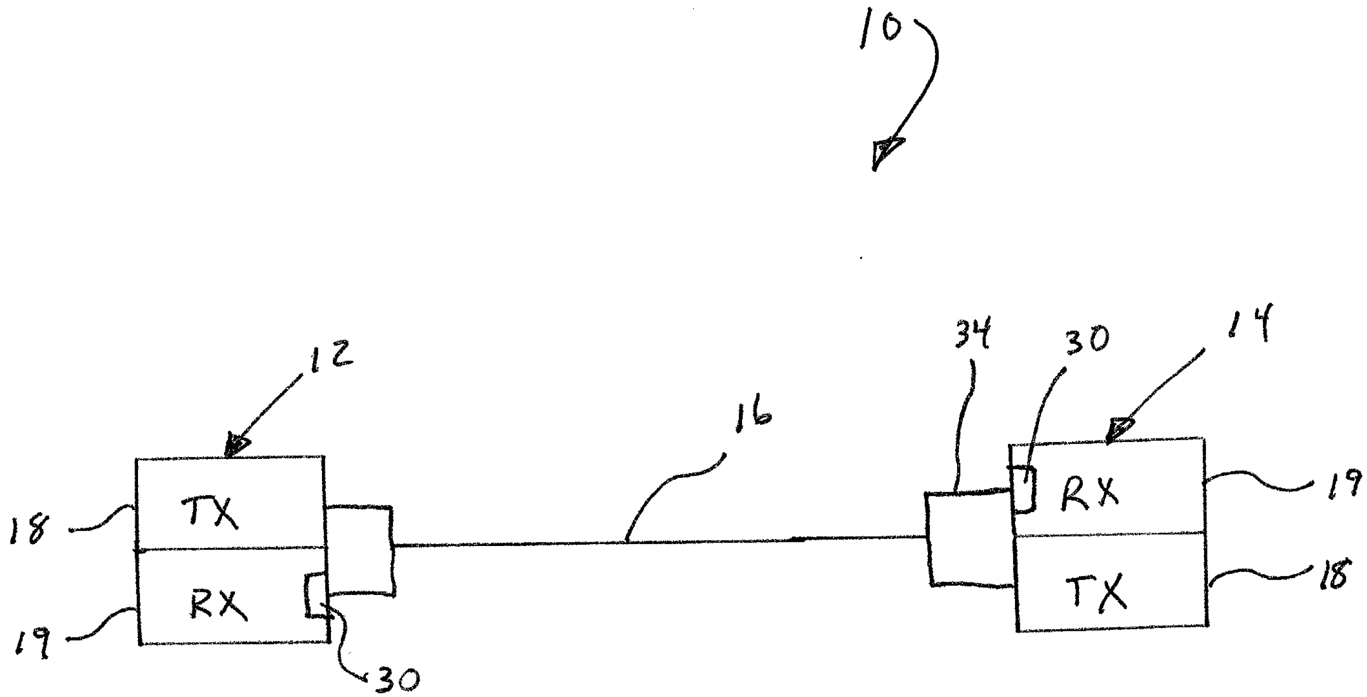

FIGURE 1

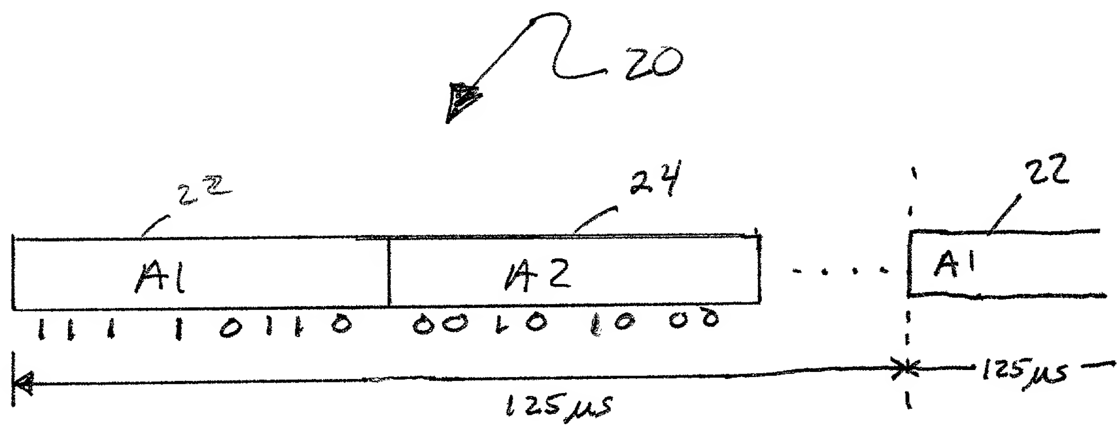

FIGURE 2

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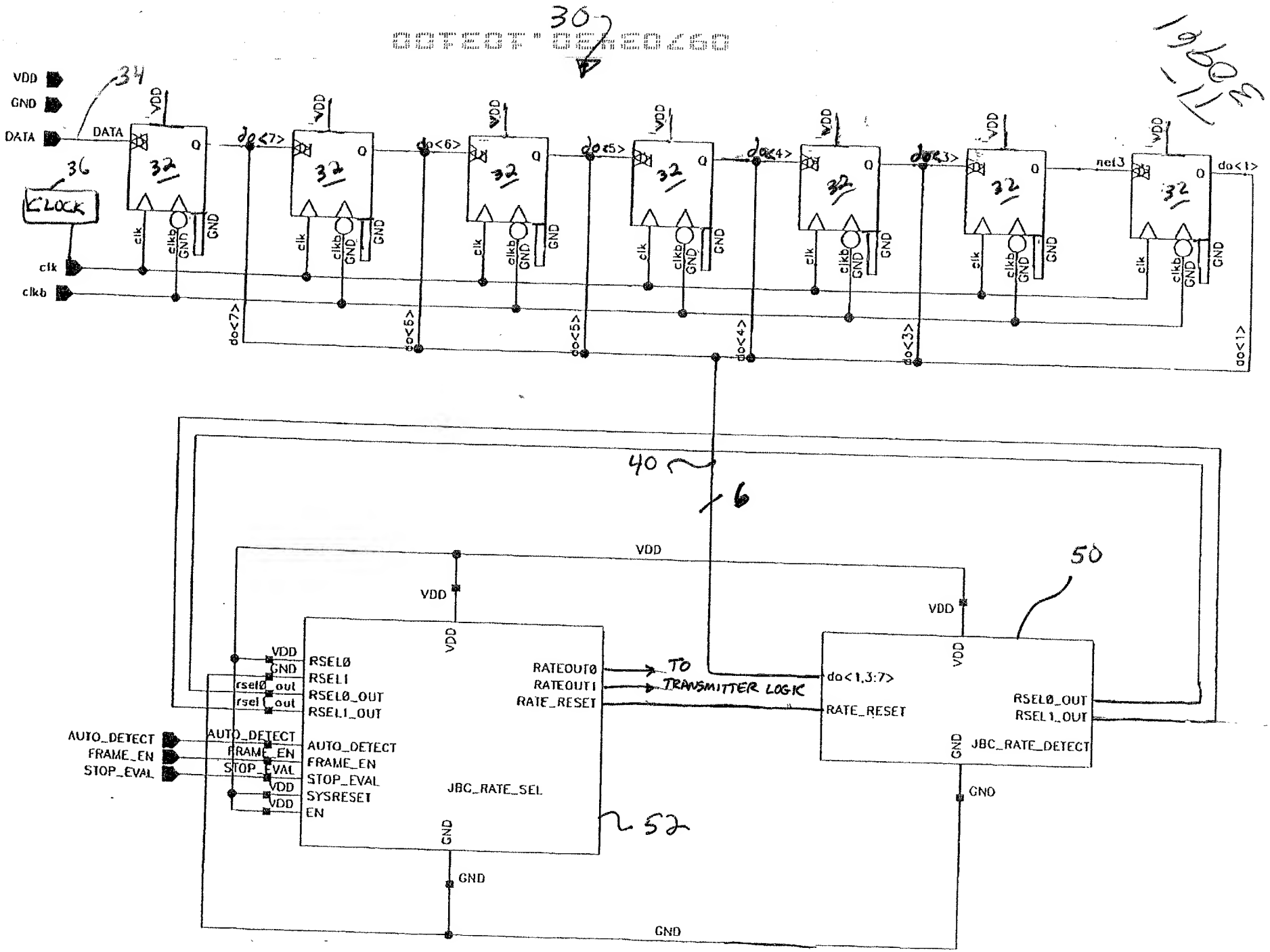
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34
36
VDD
GND
DATA
CLOCK
clk
clkb
32
do<7>
do<6>
do<5>
do<4>
do<3>
net3
do<1>
40
6
50
52
RSEL0
RSEL1
RSEL0_OUT
RSEL1_OUT
AUTO_DETECT
FRAME_EN
STOP_EVAL
SYSRESET
EN
JBC_RATE_SEL
RATEOUT0
RATEOUT1
RATE_RESET
TO TRANSMITTER LOGIC
do<1,3:7>
JBC_RATE_DETECT

FIGURE 3

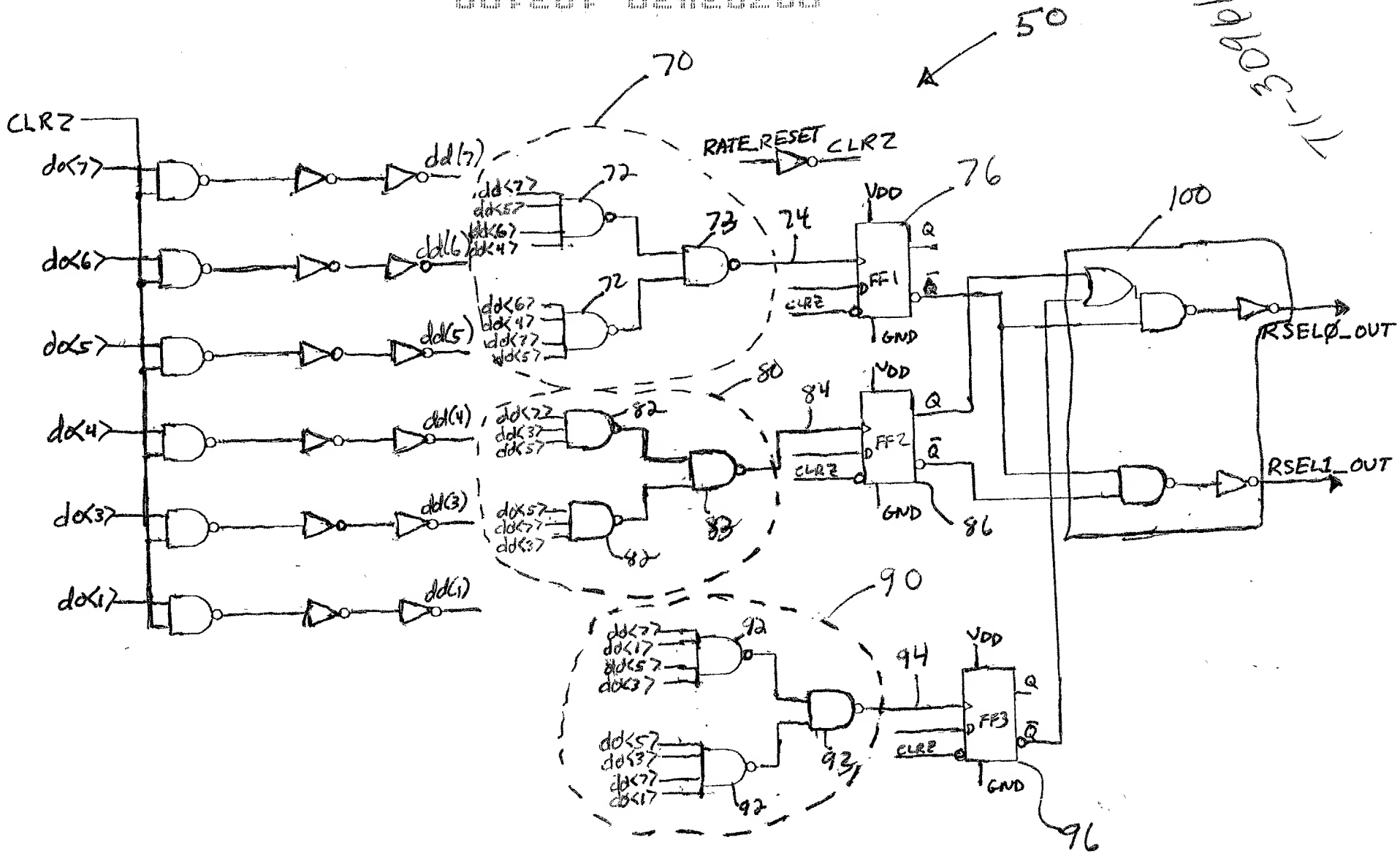


FIGURE 4

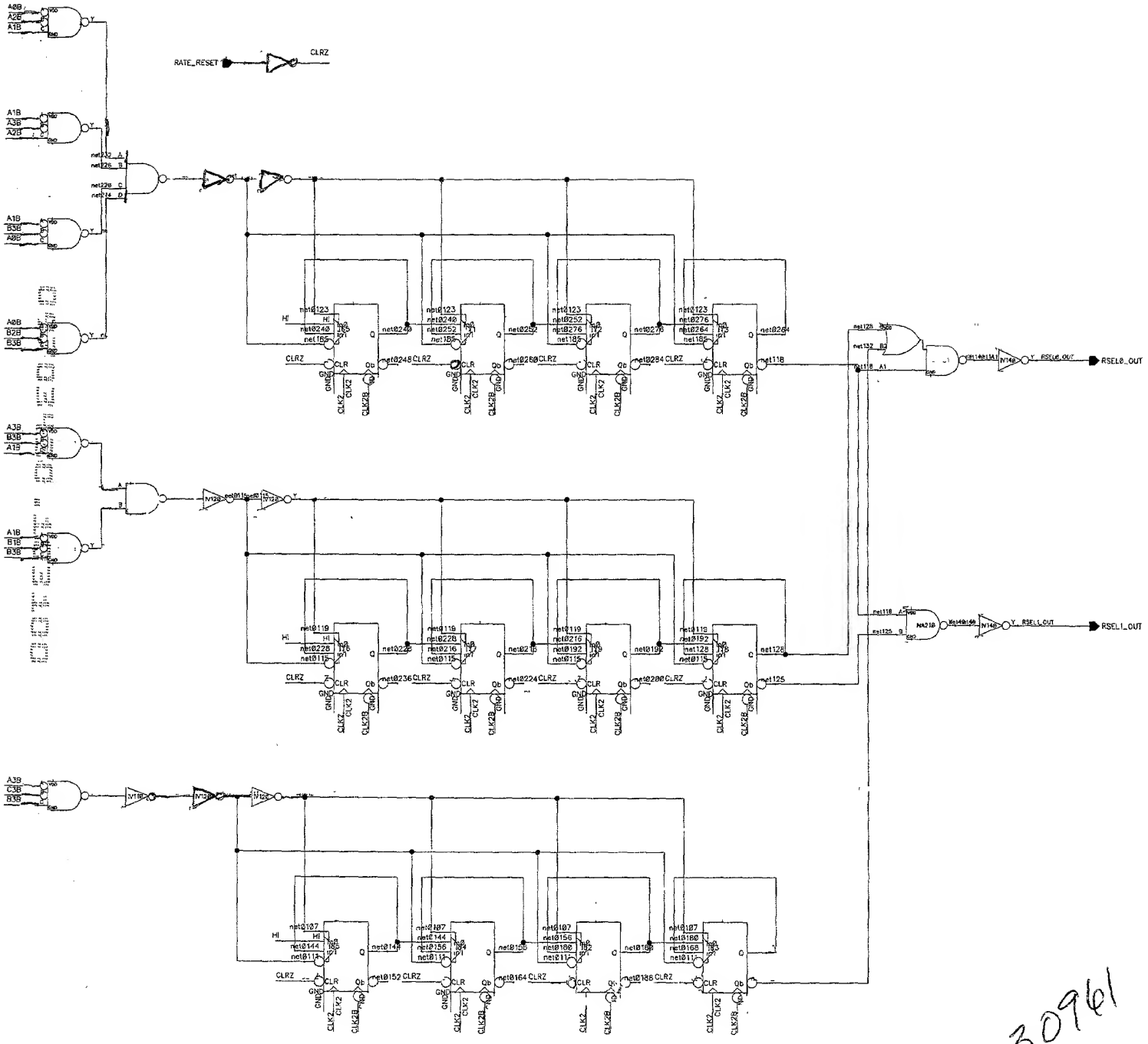
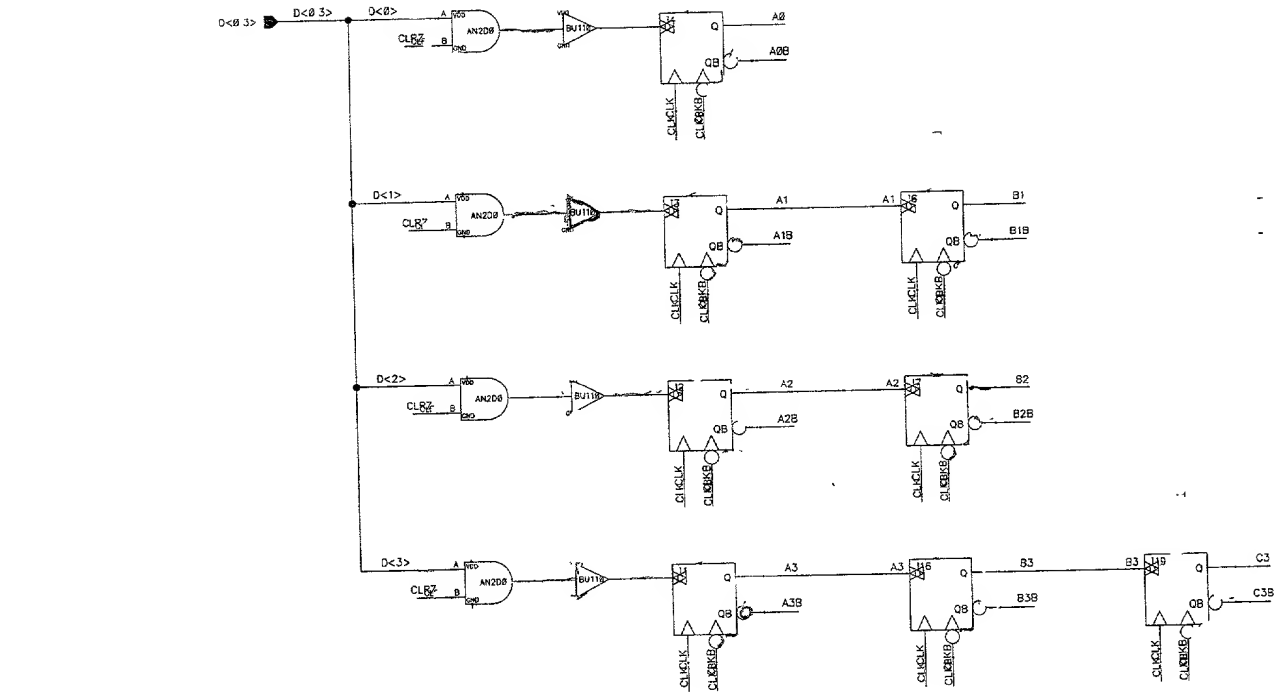


FIGURE 5
(page 1 of 2)

TI-30961



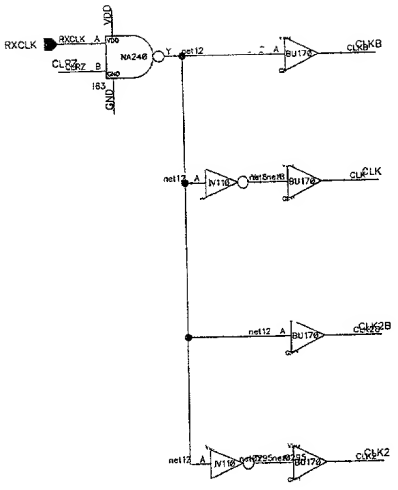


FIGURE 5
(page 2 of 2)

T1-30961

ATTORNEY'S DOCKET NO.

TI-30961

APPLICATION FOR UNITED STATES PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, section 1.56(a);

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

AUTOMATIC BIT-RATE DETECTION SCHEME FOR USE ON SONET TRANSCEIVER

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

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SIGNATURE OF INVENTOR: James B. Cho	SIGNATURE OF INVENTOR: Harry W. Hartjes	SIGNATURE OF INVENTOR:
DATE: 10-30-00	DATE: 10-30-2000	DATE: